REMARKS

By this Amendment, it is proposed that the Drawings and Specification be amended to overcome the Examiner's objections. Claims 1-22 remain pending in the application.

The Applicants respectfully request the Examiner to reconsider his earlier objections and rejections in light of the foregoing amendments and the following remarks.

Objection to the Specification

The Applicant has included herein a new Abstract of the Disclosure to overcome the Examiner's objection.

The Examiner made an objection to the disclosure, page 9, because the disclosure did not detail "what the various labels within the equations represent".

The Specification is amended herein at page 10 to address the Examiner's concern. The recited equations are standard engineering equations representing the amount of charge in the inversion layer and therefore do not constitute new matter. W represents the width of the inversion layer. L represents the length of the inversion layer. C_{ox} represents the capacitance of a unit area of the oxide layer. As such, adding their description to the disclosure does not raise the issue of adding new matter to the Specification.

Section 112 rejection of Claims 13-17 and 20

Claims 13-17 and 20 were rejected under 35 USC 112, first paragraph. The Applicant respectfully traverses the rejection.

The circuit shown in Figs. 7 and 8 is not to be taken as existing alone, but is to be taken as belonging to a larger circuit. Any IC is made up of multiple transistors. Current flowing from one transistor flows to the next, thus providing current to the next component in the circuit path. One of ordinary skill in the art would understand that any current source can be used for current source 740 of the circuit shown in Figs. 7 and 8. Basic engineering principles of

charging the current source apply. One of ordinary skill in the art would understand a voltage potential across a capacitive current source stores energy to be released by a current path.

Claims 13-17 and 20 are in full conformance with 35 USC 112. It is therefore respectfully requested that the rejection be withdrawn.

Alleged Anticipation of claims 1-5, 8-10, 12, 18, 19, 21 and 22 in view of Hartson.

In the Office Action, claims 1-5, 8-10, 12, 18, 19, 21 and 22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by US Patent No. 5,343,196 to Harston ("Harston"). The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10, 12, 18, 19, 21 and 22 of the present application recite, *inter alia,* a transistor switch and a pull-down mirror path that operate to substantially continuously to reduce charge injection flowing to a load.

Harston appears to teach a method of reducing the amount of current switched to a reference line so as to reduce the overall power consumption of a digital to analog converter (DAC). To achieve this, three transistors are employed. One MOS transistor acts as a current source. The two other transistors act alternatively to direct current to either the load or ground (Harston, col. 1, line 41-42).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently, in a single prior art reference. Verdegaal Bros. v . Union Oil Co. of California , 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); Richardson v . Suzuki Motor Co ., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); In re Bond , 15 USPQ2d 1566 (Fed. Cir. 1990); *See* also MPEP §2131.

Harston fails to disclose a transistor switch and a pull-down mirror path operating to substantially continuously reduce charge injection flowing to a load. Harston's alternative parallel path flows current to ground, not the capacitor 10pF as stated by the Examiner on page 5 of the Office Action. As seen in Harston's Fig. 3, the alternative path for the current coming from MP1 is to

analog ground AGND, not to a load. Harston does not provide a substantially continuous flow of current to a load while reducing charge injection.

Accordingly, for at least all the above reasons, claims 1-5, 8-10, 12, 18, 19, 21 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Alleged Obviousness of claims 6, 7 and 11 over Harston and further in view of the Applicant's prior art.

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103 as allegedly being obvious over Harston and further in view of the compensated transistor switch of the Applicant's prior art Fig. 3. The Applicant respectfully traverses the rejection.

Claims 6, 7 and 11 recite, *inter alia,* a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

As discussed above, Harston fails to teach a transistor switch and a pull-down mirror path operate to substantially continuously reduce charge injection flowing to a load. The Office Action correctly notes that Harston also fails to teach or suggest a compensated transistor switch made up of three transistors.

However, the Office Action relies on Applicant's prior art Fig. 3 to teach a three transistor compensated transistor switch (Office Action page 6). Using this, the Examiner alleges that it would have therefore been obvious to combine the teachings of Harston and Applicant's prior art to create a current switch to reduce charge injection (Office Action page 6). The Applicant respectfully disagrees.

It is Applicant's belief, but not knowledge, that the circuit shown in Fig. 3 may be prior art. The circuit shown in Fig. 3 may not be prior art.

Even a combination of Harston and the Applicant's prior art (assuming that Fig. 3 is prior art) would still fail to teach or suggest every claim limitation of claims 6, 7 and 11. In particular, neither Harston not Applicant's prior

art teach a transistor switch and a pull-down mirror path operating to substantially continuously reduce charge injection flowing to a load.

The Applicant's prior art teaches a three transistor compensated circuit. A three transistor compensated circuit is not a transistor and a pull-down mirror path, as claimed by claims 6, 7 and 11. Accordingly, even a combination of Harston and Applicant's prior art would fail to suggest or teach a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

It is respectfully submitted that claims 6, 7 and 11 are patentable over the prior art of record for at least the reasons given above. Accordingly, Applicants respectfully request withdrawal of the foregoing rejection.

Alleged Obviousness of claims 13-17 and 20 over Harston.

In the Office Action, claims 13-17 and 20 were rejected under 35 U.S.C. §103 as allegedly being obvious over Harston. The Applicants respectfully traverse the rejection.

Claims 13-17 and 20 recite, *inter alia*, a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

As stated above, Harston fails to teach or suggest a transistor switch and a pull-down mirror path operating to substantially continuously reduce charge injection flowing to a load, as claimed by claims 13-17 and 20. The Office Action correctly notes that Harston fails to teach or suggest a pull-up amplifier.

However, the Office Action alleges that it would have been obvious to one of ordinary skill in the art to have modified the circuit of Fig. 3 by reversing the polarities and transistor types (Office Action, page 7). The Applicant respectfully disagrees.

Reversing the polarities and transistor types of Fig. 3 would still fail to teach or suggest every claim limitation of claims 13-17 and 20. In particular, reversal of polarities and transitor types does not teach a transistor switch and a

pull-down mirror path operating to substantially continuously reduce charge injection flowing to a load.

Accordingly, for at least all the above reasons, claims 13-17 and 20 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-22 are patentable over the prior art of record.

All rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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